IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

TAE-SUNG KIM

Serial No.:	10/767,281	Examiner:	WARREN, MATTHEW E.
Filed:	30 January 2004	Art Unit:	2815

For: NOVEL CONDUCTIVE ELEMENTS FOR THIN FILM TRANSISTORS USED IN A FLAT PANEL DISPLAY

INFORMATION DISCLOSURE STATEMENT

Paper No. 7

Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites, describes and provide copies of the following art references. Under 37 C.F.R. §1.98(a)(2) however, copies of U.S. patent reference(s) are not provided.

1. U.S. Patent No. 6,180,511 to Kim *et al.*, entitled *METHOD FOR FORMING INTERMETAL DIELECTRIC OF SEMICONDUCTOR DEVICE* issued on January 30, 2001;

2. U.S. Patent No. 6,674,502 to Terakado *et al.*, entitled *LIQUID CRYSTAL DISPLAY WITH NITRIDED INSULATING SUBSTRATE FOR TFT*, issued on January 6, 2004;

3. U.S. Patent No. 6,642,093 to Kubo *et al.*, entitled *METHOD FOR MANUFACTURING A SEMICONDUCTOR DEVICE*, issued on November 4,

2003;

4. U.S. Patent No. 6,608,353 to Miyazaki *et al.*, entitled *THIN FILM TRANSISTOR HAVING PIXEL ELECTRODE CONNECTED TO A LAMINATE STRUCTURE*, issued on August 19, 2003;

5. U.S. Patent No. 6,534,393 to Zhou *et al.*, entitled *METHOD FOR FABRICATING LOCAL METAL INTERCONNECTIONS WITH LOW CONTACT RESISTANCE AND GATE ELECTRODES WITH IMPROVED ELECTRICAL CONDUCTIVITY*, issued on March 18, 2003;

6. U.S. Patent No. 6,518,630 to You *et al.*, entitled *THIN FILM TRANSISTOR ARRAY SUBSTRATE FOR LIQUID CRYSTAL DISPLAY AND METHOD FOR FABRICATING SAME*, issued on February 11, 2003;

7. U.S. Patent No. 6,410,986 to Merchant *et al.*, entitled *MULTI-LAYERED TITANIUM NITRIDE BARRIER STRUCTURE*, issued on June 25, 2002;

8. U.S. Patent No. 6,380,625 to Pramanick *et al.*, entitled *SEMICONDUCTOR INTERCONNECT BARRIER AND MANUFACTURING METHOD THEREOF*, issued on April 30, 2002;

9. U.S. Patent No. 6,365,927 to Cuchiaro *et al.*, entitled *FERROELECTRIC INTEGRATED CIRCUIT HAVING HYDROGEN BARRIER LAYER*, issued on April 2, 2002;

10. U.S. Patent No. 6,309,965 to Matshitsch *et al.*, entitled *METHOD OF*

PRODUCING A SEMICONDUCTOR BODY WITH METALLIZATION ON THE BACK SIDE THAT INCLUDES A TITANIUM NITRIDE LAYER TO REDUCE WARPING, issued on October 30, 2001;

11. U.S. Patent No. 6,224,942 to Leiphart, entitled *METHOD OF FORMING AN ALUMINUM COMPRISING LINE HAVING A TITANIUM NITRIDE COMPRISING LAYER THEREON*, issued on May 1, 2001;

12. U.S. Patent No. 6,096,572 to Nakamura, entitled *MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE WITH LOW CONTACT RESISTANCE BETWEEN TRANSPARENT ELECTRODE AND PAD ELECTRODE*, issued on August 1, 2000;

13. U.S. Patent No. 5,759,916 to Hsu *et al.*, entitled *METHOD FOR FORMING A VOID-FREE TITANIUM NITRIDE ANTI-REFLECTIVE COATING (ARC) LAYER UPON AN ALUMINUM CONTAINING CONDUCTOR LAYER*, issued on June 2, 1998;

14. U.S. Patent No. 5,341,026 to Harada *et al.*, entitled *SEMICONDUCTOR DEVICE HAVING A TITANIUM AND A TITANIUM COMPOUND MULTILAYER INTERCONNECTION STRUCTURE*, issued on August 23, 1994;

15. U.S. Patent No. 4,976,839 to Inoue, entitled *METHOD OF FORMING A BARRIER LAYER BETWEEN A SILICON SUBSTRATE AND AN ALUMINUM ELECTRODE OF A SEMICONDUCTOR DEVICE*, issued on December 11, 1990;

16. U.S. Patent No. 4,933,296 to Parks *et al.*, entitled *N^+ AMORPHOUS SILICON THIN FILM TRANSISTORS FOR MATRIX ADDRESSED LIQUID CRYSTAL DISPLAYS*, issued on June 12, 1990;

17. U.S. Patent No. 4,910,580 to Kuecher *et al.*, entitled *METHOD FOR MANUFACTURING A LOW-IMPEDANCE, PLANAR METALLIZATION COMPOSED OF ALUMINUM OR OF AN ALUMINUM ALLOY*, issued on March 20, 1990;

18. U.S. Patent No. 4,778,258 to Parks *et al.*, entitled *PROTECTIVE TAB STRUCTURE FOR USE IN THE FABRICATION OF MATRIX ADDRESSED THIN FILM TRANSISTOR LIQUID CRYSTAL DISPLAYS*, issued on October 18, 1998;

19. U.S. Patent No. 4,646,424 to Parks *et al.*, entitled *DEPOSITION AND HARDENING OF TITANIUM GATE ELECTRODE MATERIAL FOR USE IN INVERTED THIN IFILM FIELD EFFECT TRANSISTORS*, issued on March 3, 1987; and

20. U.S. Patent No. 4,511,756 to Moeller *et al.*, entitled *AMORPHOUS SILICON SOLAR CELLS AND A METHOD OF PRODUCING THE SAME*, issued on April 16, 1985.

21. Japanese Patent Publication No. 09-213656 to Ishida, entitled *SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING IT*, published on August 15, 1997;

22. Japanese Patent Publication No. 04-265757 to Kawasaki, entitled *THIN FILM TYPE THERMAL HEAD*, published on September 21, 1992; and

23. Japanese Patent Publication No. 2002-26335 to Yaegashi, entitled *THIN FILM TRANSISTOR AND METHOD OF MANUFACTURING THEREOF*, published on 25 January 2002.

Kim *et al.* '511 relates to a method for forming internetal dielectric of semiconductor device for reducing chemical mechanical polishing process time.

Terakado *et al.* '502 discloses "a liquid crystal display comprising ... a conductive layer formed over said protective layer, said conductive layer including a metallic element; a lower conductive layer provided between said surface and said conductive layer, said lower conductive layer having said metallic element and nitrogen atoms; and an upper conductive layer provided above said conductive layer; said upper conductive layer having said metallic element and nitrogen atoms; wherein said protective layer has a nitrogen concentration of about 10 mol % or more at said surface."

Kubo *et al.* '096 discloses "forming a film of aluminum sandwiched by films of titanium nitride on said third interlayer insulation film, and patterning said film of aluminum."

Miyazaki *et al.* '353 discloses "an electronic circuit formed on an insulating substrate and having thin-film transistors (TFTs) comprising semiconductor layers." The thickness of the semiconductor layer is less than 1500 ANG, *e.g.*, between 100 and 750 ANG. A first layer consisting mainly of titanium and nitrogen is formed on the semiconductor layer. A second layer consisting of aluminum is formed on top of the first layer. The first and second layers are patterned into conductive interconnects. The bottom surface of the second layer is substantially

totally in intimate contact with the first layer.

Zhou *et al.* '393 discloses in claim 8 that, "the method of claim 1, wherein said metal layer is a multilayer composed of a titanium/titanium nitride barrier layer and an upper layer of aluminum-copper alloy."

You *et al.* '630 (Samsung Electronics Co., Ltd.) discloses "the thin film transistor array substrate of claim 1, wherein the intermetallic compound layer is formed of aluminum-molybdenum alloy, aluminum-titanium alloy, aluminum-tantalum alloy, or aluminum0chrome alloy."

Merchant *et al.* '986 discloses that "a titanium nitride barrier within an integrated contact structure is formed as a multi-layered stack."

Pramanick *et al.* '625 discloses that "the combination of the titanium nitride layer and the second barrier material provide a superior barrier for conductive material layers, such as, copper/coppre layers, and copper/aluminum layers."

Cuchiaro *et al.* '927 discloses "a hydrogen diffusion barrier in an integrated circuit is located to inhibit diffusion of hydrogen to a thin film of metal oxide material in an integrated circuit." The hydrogen diffusion barrier comprises at least one of the following nitrides: aluminum titanium nitride (Al.sub.2 Ti.sub.3 N.sub.6), aluminum silicon nitride (Al.sub.2 Si.sub.3 N.sub.6), aluminum niobium nitride (AlNb.sub.3 N.sub.6), alumnum tantalum nitride (AlTa.sub.3 N.sub.6), aluminum copper nitride (Al.sub.2 Cu.sub.3 N.sub.4), tungsten nitride (WN), and copper nitride (CDu.sub.3 N.sub.2).

Matschitsch *et al.* '965 discloses that "on a silicon semiconductor body an aluminum

layer and a diffusion barrier layer that includes titanium are provided." A titanium nitride layer is incorporated into the titanium layer because it has been demonstrated that the titanium nitride layer can compensate for a large proportion of the wafer warping that occurs. Matschitsch '965 also has U.S. Patent No. 6,147,403 that discloses that "on a silicon semiconductor body an aluminum layer and a diffusion barrier layer that includes titanium are provided."

Leiphart '942 discloses in claim 1 that, "a method of forming an aluminum comprising line having a titanium nitride comprising layer ... ."

Nakamura '572 discloses that "in a semiconductor device such as a thin film transistor ... the protection layer may be formed of titanium or a laminate layer of a titanium layer and a titanium nitride layer."

Hsu *et al.* '916 discloses in claim 8 that, "the method of claim 7 wherein: the titanium rich titanium nitride layer has a thickness of from about 10 to about 200 angstroms; the substantially stoichiometric titanium nitride layer has a thickness of from about 50 to about 1500 angstroms; and the titanium rich titanium nitride layer promotes adhesion of the substantially stoichiometric titanium nitride layer to the aluminum containing conductor layer."

Harada *et al.* '026 discloses that "the second aluminum interconnection layer includes a titanium layer, a titanium nitride layer and an aluminum alloy layer."

Inoue '839 discloses that "a titanium nitride barrier layer of 50 to 200 nm in thickness is fabricated between a silicon substrate and an aluminum electrode layer of an IC device."

Parks *et al.* '296 discloses in claim 1 that, "a process for the fabrication of thin film field

effect transistors in active matrix liquid crystal display devices, said process comprising the sequential steps of: disposing a gate metallization layer pattern on a portion of a first major surface of an insulative substrate, said gate metal comprising titanium, said pattern including gate electrodes."

Kuecher *et al.* '580 discloses that "to improve the planarization and reliability of low-impedance aluminum metallizations, a substrate provided with a titanium/titanium nitride double layer diffusion barrier layer and having a contact hole is provided or, respectively, filled with an aluminum/silicon alloy sandwich structure composed of a sequence of n aluminum/silicon layers having n-1 intermediate layers of titanium applied thereon, whereby the layer thickness ratio of the titanium intermediate layers to the overall layer thickness d of the metallization behaves like 1:10."

Parks *et al.* '258 discloses in claim 9 that, "the fabrication process of claim 1 in which said source and drain metallization comprises aluminum."

Parks *et al.* '424 discloses in claim 1 that, "a method for deposition of gate electrode material in an inverted thin film field effect transistor, said method comprising the steps of: disposing a layer of silicon oxide on an insulative substrate; disposing a layer of titanium over said silicon oxide layer; coating said titanium layer with a positive photoresist."

Moeller *et al.* '756 discloses "solar cells having a semiconductor body composed of amorphous silicon which is deposited on a substrate coated with aluminum at least on one of its surfaces, with a diffusion barrier layer composed of titanium nitride positioned between the aluminum layer and the semiconductor body."

Ishida '656 relates to the structure and its manufacturing method of the conductive layer

formed in the side attachment wall of opening formed in the interlayer insulation film. English language Abstract is attached.

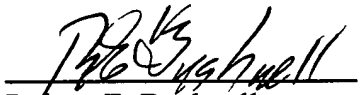
Kawasaki '757 relates to a thin film type thermal head having high reliability by preventing breaking of wire caused by energizing a power feed layer. English language Abstract is attached.

Yaegashi '335 discloses that a thin film transistor and the method of manufacturing thereof, which enables at least either the gate electrode or the source drain electrode to be formed of Al and high-melting metal so as to decrease thin film transistor resistance and to prevent a high-resistance layer from being formed by mutual diffusion caused by heat at an interface between Al and high-melting metal, where the thin film transistor is mainly used as a switching device of a liquid crystal display device.

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

A fee of $180.00 is incurred by filing of the present information disclosures statement. Applicant's check drawn to the order of Commissioner is attached herewith. Should the check become lost, be deficient in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



Robert E. Bushnell
Reg. No.: 27,774

1522 "K" Street, N.W., Suite 300
Washington, D.C. 20005
Area Code: (202) 408-9040

Folio: P57002
Date: 7/13/05
I.D.: REB/kf

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Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
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FEE TRANSMITTAL

Patent fees are subject to annual revision.

Complete If Known	
Application Number	10/767281
Filing Date	30 January 2004
First Named Inventor	Tae-Sung KIM
Examiner Name	Matthew WARREN
Group/Art Unit	2815
Attorney Docket No.	P57002

TOTAL AMOUNT OF PAYMENT	($) 180.00

METHOD OF PAYMENT (check one)

1. ■ **Payment Enclosed: (CHECK #49348)**

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❑ Charge Any Additional Fee Required Under 37 C.F.R. §1.16 and 1.17.

❑ Applicant claims small entity status. See 37 CFR 1.27

2. ■ The Commissioner is hereby authorized to charge any deficiency and credit any over payments to:

Deposit Account Number: 02-4943

FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
				EXTENSION OF TIME FEES	
1251	120	2251	60	Extension for reply within first month	$
1252	450	2252	225	Extension for reply within second month	$
1253	1020	2253	510	Extension for reply within third month	$
1254	1590	2254	795	Extension for reply within fourth month	$
1255	2160	2255	1080	Extension for reply within fifth month	$
				APPEAL	
1401	500	2401	250	Notice of Appeal	$
1402	500	2402	250	Filing a brief in support of an appeal	$
1403	1000	2403	500	Request for oral hearing	$
				CLAIMS	
1201	200	2201	100	Independent claims in excess of 3	$
1202	50	2202	25	claims in excess of 20 (4)	$
Other Fee (specify)					$
Other Fee (specify)					$
Other Fee (specify)					$

FEE CALCULATION

Fee Code	Fee ($)	Fee Code	Fee ($)	Fee Description	Fee Paid
				MISCELLANEOUS	
1801	$790	2801	$395	Request for continued examination (RCE)	$
1806	$180			Submission of an IDS	$180.00
1814	$130	2814	$65	Statutory disclaimer	$
8021	$40			Recordation of assignment per property	$
				TRADEMARK	
6001/7001		$335		Application for registration, per class	$
6002/7002		$100		Amendment to Allege Use, per class	$
6003/7003		$100		Statement of Use, per class	$
6004/7004		$150		Request for six-month extension of time, per class	$
6205/7205		$100		§8 affidavit, per class	$
6208/7208		$200		§15 affidavit, per class	$
6201/7201		$400		Application for renewal, per class	$
6403/7403		$100		Ex parte appeal, per class	$
				PETITION	
1462		$400		Petitions to Director (Group I)	$
1463		$200		Petitions to Director (Group II)	$
1464		$130		Petitions to Director (Group III)	$
1452	$500	2452	$250	Petitions to revive unavoidably abandoned application	$
1453	$1500	2453	$750	Petitions to revive unintentionally abandoned application	$
				PATENT MAINTENANCE	
1551	$900	2551	$450	Due at 3.5 years	$
1552	$2300	2552	$1150	Due at 7.5 years	$
1553	$3800	2553	$1900	Due at 11.5 years	$
Other Fee (specify)					$
Other Fee (specify)					$
Other Fee (specify)					$

SUBTOTAL: LEFT COLUMN	$.00	SUBTOTAL: RIGHT COLUMN	$180.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	Robert E. Bushnell, Esq.			Reg. Number	27,774
Signature	/Robert E. Bushnell/	Date	13 July 2005	Deposit Account User ID	

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INFORMATION DISCLOSURE STATEMENT PTO-1449 (PAGE 1 OF 2)	SERIAL NUMBER 10/767,281	DOCKET NO. P57002
	APPLICANT TAE-SUNG KIM	
	FILING DATE 30 January 2004	GROUP 2815

U.S. PATENT DOCUMENTS

EXAMINER	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,180,511	1/01	Kim et al.			
	6,674,502	1/04	Terakado et al.			
	6,642,093	11/03	Kubo et al.			
	6,608,353	8/03	Miyazaki et al.			
	6,534,393	3/03	Zhou et al.			
	6,518,630	2/03	You et al.			
	6,410,986	6/02	Merchant et al.			
	6,380,625	4/02	Pramanick et al.			
	6,365,927	4/02	Cuchiaro et al.			
	6,309,965	10/01	Matschitsch et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	JP09-213656	8/97	Japan			Abstract	
	JP04-265757	9/92	Japan			Abstract	
	JP2002-26335	1/02	Japan			Abstract	

OTHER DOCUMENTS ***(Including Author, Title, Date, Pertinent Pages, etc.)***

EXAMINER: *DATE CONSIDERED:*

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT
PTO-1449 (PAGE 2 OF 2)

SERIAL NUMBER 10/767,281	DOCKET NO. P57002
APPLICANT TAE-SUNG KIM	
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE
	6,224,942	5/01	Leiphart			
	6,096,572	8/00	Nakamura			
	5,759,916	6/98	Hsu et al.			
-	5,341,026	8/94	Harada et al.			
	4,976,839	12/90	Inoue			
-	4,933,296	6/90	Parks et al.			
	4,910,580	3/90	Kuecher et al.			
	4,778,258	10/88	Parks et al.			
	4,646,424	3/87	Parks et al.			
	4,511,756	4/85	Moeller et al.			

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

OTHER DOCUMENTS ***(Including Author, Title, Date, Pertinent Pages, etc.)***

EXAMINER: *DATE CONSIDERED:*

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